esteem3

Enabling Science through European Electron Microscopy

Report on protocols for achieving low resistive FE(I)BID Ohmic contacts

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Introduction

TEM is the most appropriate tool to measure *in-situ* local electric fields in thin films and working devices. Apart from nanometre spatial resolution, TEM allows the study of individual devices, thus providing crucial information to microelectronics manufacturers for the development and optimization of (future) devices in terms of reliability, speed and power consumption. However, few investigations on real devices in operation had been performed using electron microscopy before the start of ESTEEM3. The main limitation was the preparation of suitable samples for operando experiments that allow reliable comparisons with conventional electrical characterisation of the on-chip devices.

During ESTEEM3, protocols have been developed to prepare specimens suitable for in-situ biasing experiments (D6.1) on thin films [1] or devices [2]. A lamella is extracted from the thin-film sample or device by focused ion beam (FIB) and transferred to specially designed chips with lithographically patterned electrodes. These chips are in turn inserted into dedicated sample holders for the TEM. Care is taken to minimising artefacts due to the ion-beam thinning process, in particular surfaces effects, and to maintain the quality of the electrical contacts. These samples are extremely fragile, both electrically and mechanically, and different steps were required to optimise the success rate of experiments. In particular, it is of paramount importance that the contacting be of the highest quality: with the lowest possible contact resistance. Otherwise, the locally applied bias will not correspond to the applied external bias.

Here we give a report on the progress achieved during the ESTEEM3 project towards this objective.

Protocol for low resistive FE(I)BID Ohmic contacts

A complete and detailed protocol has been developed by STU [3]. The primary objective was to develop a FIB sample-preparation routine for in-situ electrical measurements, with a minimal number of attachment/detachment steps and a reduced use of fixation with Pt (Fig. 1). Also, the size of Pt contacts needed to be controlled, where all contacts on one chip should have the same size and the same thickness. The aim was for a lamellae preparation procedure that will result in contamination-free and artefact-free electron-transparent samples. In addition, the effect of different parameters used during the sample preparation and of the geometry of the lamellae on the electrical measurements should be fully characterised.

The methodology developed consists of the following steps [3]:

1. *Pt protection layer*. Deposition of a protective Pt layer at the region of interest. The size of the Pt layer should be determined based on the experimental requirements. We recommend measuring the distance between the electro-des on the MEMS chips before depositing the protective Pt layer. For our application on a FIB-optimized E-chip, the protective Pt layer with the size of 25 µm × 4 µm × 1 µm was deposited by ion beam deposition at 30 kV and 0.5 nA at a stage tilt angle of 52° (Fig. 2a).

2. *Milling*. Trenches of material to be milled on both sides parallel to the Pt layer (Figs. 2a, 2b). Extra space should be ensured and left on one end of the Pt layer, since the lamella lift-out is done in an alternative geometry com-pared with the regular lift-out procedure. For the samples presented here, milling was done at an ion-beam energy of 30 kV in several consecutive steps, starting with a beam current of 15 nA at a tilt angle of 52°with the regular cross-section pattern (RCS) (Fig. 2a, area marked with orange rectangles). For further thinning the beam current was reduced to 3 and 1 nA, re-spectively, at an over-tilt of 1.5°, using the cleaning cross-section (CCS) (Fig. 2a, area marked with yellow rectangles). The final trench thicknesses were 1, 1.5, and 2 µm, respectively (Fig. 2b).

3. *U-cut*. Cut the sample with three rectangular patterns forming a U-shape, while the stage is tilted to 7°, to separate it from the bulk material.

4. *Lift out*. Rotate the sample by 90° in clockwise direction while keeping the stage tilt at 0°, so that the Pt layer and the lamella are in a vertical direction (Fig. 2c). It is important to keep the side with more space between the Pt strap and the surrounding bulk sample on the bottom side. For our method, it is essential that a precisely shaped, pencil-like micromanipulator needle is used. The size of the needle tip should not exceed the thickness of the lamella. Carefully insert the micromanipulator needle and attach it with Pt at the top side of the lamella. Cut the contact between the lamella and the bulk material, and completely lift out the lamella (Figs. 2d, 2e). Note that due to the special geometry, it is challenging to cut this contact free, if not enough cutting area is available.

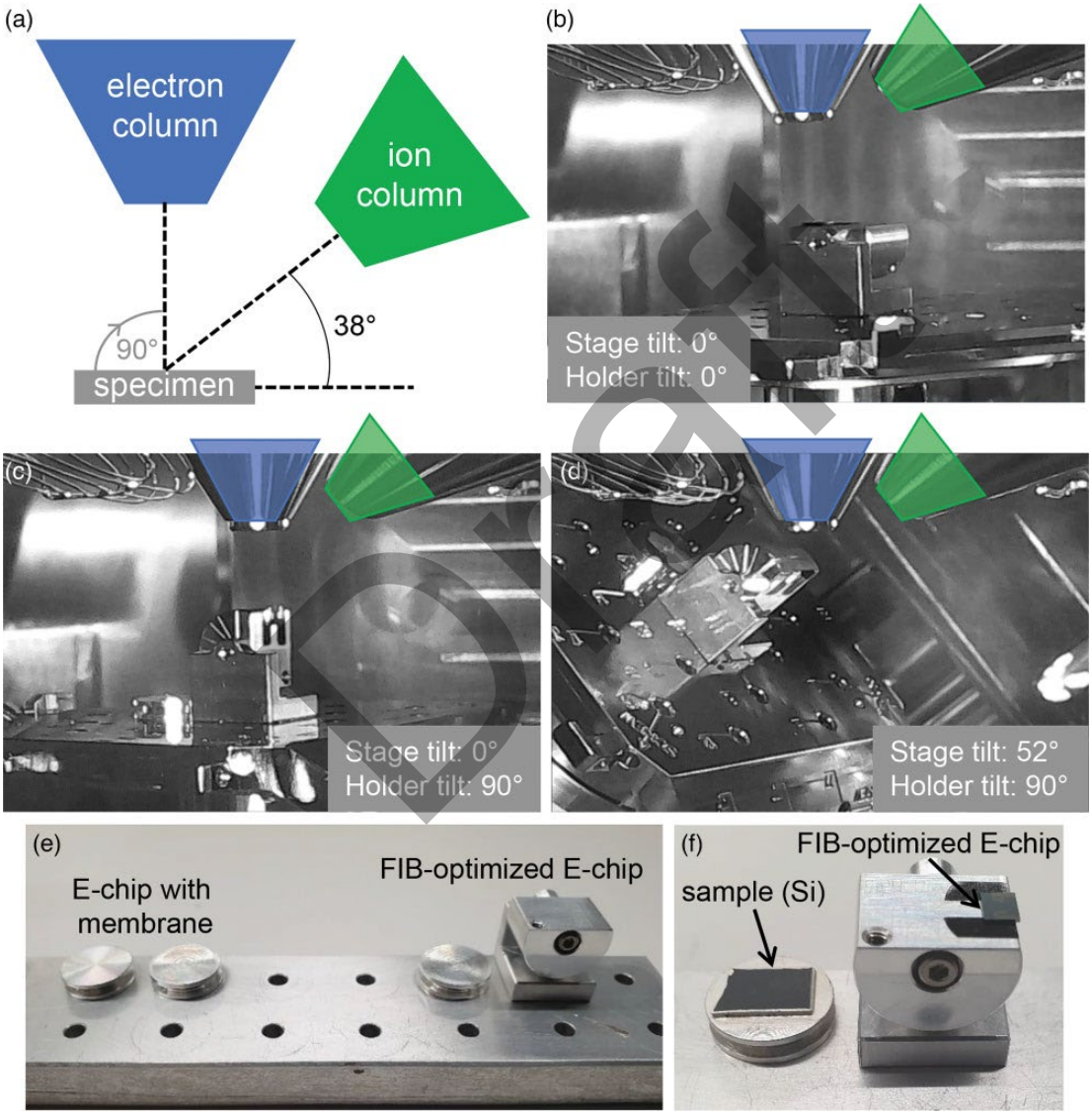

Fig. 1. Schematic diagram and geometry used for the FIB sample preparation of in-situ lamellae on a FIB-optimized E-chip (a–d). The custom flat holder and the holder with a manual tilt are used for the preparation of lamellae on E-chips with a membrane (e, left) and on the FIB-optimized E-chips (e, right and f).[3]

5. *Cleaning the backside of lamella*. This step is necessary only for lamellae that will be deposited on MEMS chips with a membrane, where the backside of lamellae cannot be cleaned after the deposition.

Rotate the micromanipulator needle for 90° in an anti-clockwise direction (Fig. 2f) and clean the backside of the lamella at 5 kV and 16 pA followed by 2 kV and 8.9 pA using the area tool.

6. *Orienting lamella for transfer to the chip*. Rotate the micromanipulator needle additionally by 90° in an anti-clockwise direction (180° in the anti-clockwise direction in total from the starting point) (Fig. 2g), and completely retract the micromanipulator needle with the lamella attached to it.

7. *Inserting the chip*. Vent the FIB chamber and insert the holder with the MEMS chip attached to it (Fig. 1b). Clean the outside surfaces of the FIB with ethanol before opening the chamber, since fine dust might drop on the surface of the chip. At this point, the chip should be in horizontal orientation (Figs. 1b, 2h). The chip could be also inserted at the start, but in the described way, we protect the surface of the chip from unnecessary contamination.

8. *Transfer lamella to the chip*. Keep the stage tilt at 0° and insert the micromanipulator needle with the lamella attached to it and carefully move it toward the chip (Fig. 2i). Ensure that the lamella comes into full contact with all four electrodes once it is landed on the chip Figs. 2j, 2k). Fix the lamella to the electrodes with the Pt straps, starting with the contact that is located diagonally across the lamella from the side where the needle is attached (Fig. 2j). The electrostatic force is strong enough to adhere the lamellae to the MEMS chip with a membrane, however, the metal contact is necessary for electrical and heating experiments to avoid drift or loss of lamellae. The micromanipulator needle should be carefully cut free while trying to preserve the electro-des minimally damaged (Figs. 2j, 2k). Finally, contact and fix the lamellae with Pt straps to all four electrodes (Fig. 2l). Since the Pt protective layer on the long upper side of the lamellae is connecting two electrodes, such contacts have to be terminated. For electrical-biasing experiments, we recommend making a small cut to all edges that could affect the measurements (Fig. 2m).

9. *Thinning/cleaning the lamellae. FIB-optimized E-chip*. We recommend performing thinning and cleaning of lamellae fixed on the FIB-optimized E-chip following a custom procedure for vertical lamellae preparation. In this geometry, one can directly observe the process of thinning on both, the front and back sides of the lamella, in the SEM image. First, remove the holder with the attached FIB-optimized E-chip from the FIB chamber and manually tilt it to 90° (Fig. 1c). Following this approach, followed by cleaning at 5 kV and 16 pA (at an over-tilt of 5°) and 2 kV and 8.9 pA (at an over-tilt of 7°) with an area tool, before inserting the sample back into the TEM. Please keep in mind that these preparation conditions must be optimized for different materials.

10. *Thinning/cleaning the lamella. Chips with membrane*. Keep the stage tilt at 0°. Since the lamellae and the chip membrane window are positioned in close proximity, thinning and cleaning of such lamellae is relatively complicated. It is impossible to produce the whole surface of the lamella equally thin and flat. In addition, the thick-ness cannot be precisely controlled. It is especially demanding to clean the edges and at the same time keep the membrane intact. For this reason, the electrical-biasing chips with pre-drilled holes were used and lamellae were fixed in a way that the edges of the lamellae were placed across the holes (Fig. 2o). The area tool was used to clean the lamella at 5 kV and 16 pA and at 2 kV and 8.9 pA. Special care was taken while cleaning the edges to ensure that the membrane stayed intact.

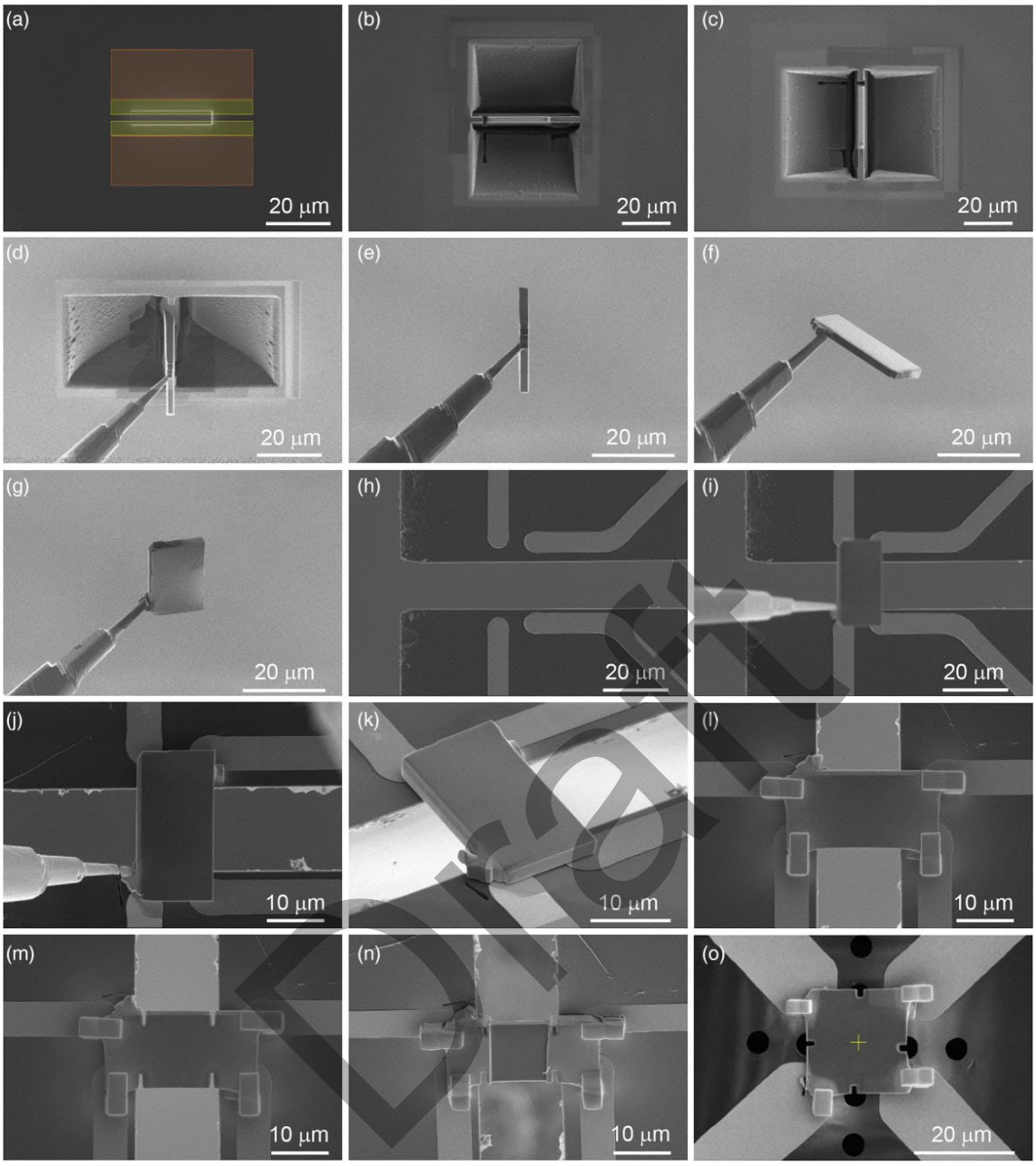

Figure 2. Methodology for preparing the lamella on an E-chip. An SEM image of the Pt protective layer with marked positions for regular (orange) and cleaning (yellow) cross-sections (a). Removal of the trenches of material on both sides of the Pt protective layer (b). After the separation of the lamella from the bulk with a U-shaped cut, rotate the sample by 90° in the clockwise direction (c). Attach the lift-out needle to the upper end of the lamella, cut free the contact between the bulk material and the lamella, and completely lift out the lamella (d, e). In the case of the FIB-optimized E-chip, rotate the micromanipulator needle with lamella attached by 180° in the anti-clockwise direction (f, g). In the case of the E-chip with a membrane, rotate the micromanipulator needle with lamellae attached to it by 90° in the anti-clockwise direction (f), clean the back side of the lamella, and rotate by another 90° in the anti-clockwise direction. Orient the E-chip (h), here, the FIB-optimized E-chip is shown. Bring the lamellae in contact with the chip, deposit one Pt contact, cut free the micromanipulator needle and deposit Pt contacts (i–l). Create cuts to avoid possible connections between the two electrodes (m). Thin the lamella (n). The lamella is prepared on the E-chip with a membrane (o). SEM images (a–c, h–o); FIB images (d–g).[3]

Electrical characterisation

The protocol for the electrical characterisation is shown in Fig. 3. After each preparation step, all samples were fully characterized. (S)TEM imaging was used to inspect the visual sample quality, while EDX-STEM measurements from several areas on the lamella were done to inspect possible contaminants (such as Pt or Ga). A typical lamella fixed on the FIB-optimized E-chip is presented in Figures 3a and 3b. Electrical four-point measurements were conducted in a stepwise manner. For each lamella, different currents were applied (50, 100, 125, and 150 µA, respectively) and the response of the sample measured.

The measurement procedure was carried out in a 3-step waveform mode: (1) increasing the current in 600 s, (2) holding the current for 200 s, and (3) decreasing the current in 600 s (Figs. 3c, 3d). In addition, alternative timings were tested, from very short exposures (60 s per step) to longer exposures (1 h per step), but no major differences could be observed. A current was applied to the upper electrodes (Figs. 3a, 3b, channel A) and the procedure was repeated in the same manner by applying the current to the bottom electrodes (Figs. 3a, 3b, channel B). Nevertheless, minor hysteresis loops occur in the current–voltage characteristic curve as the current is ramped up and down again.

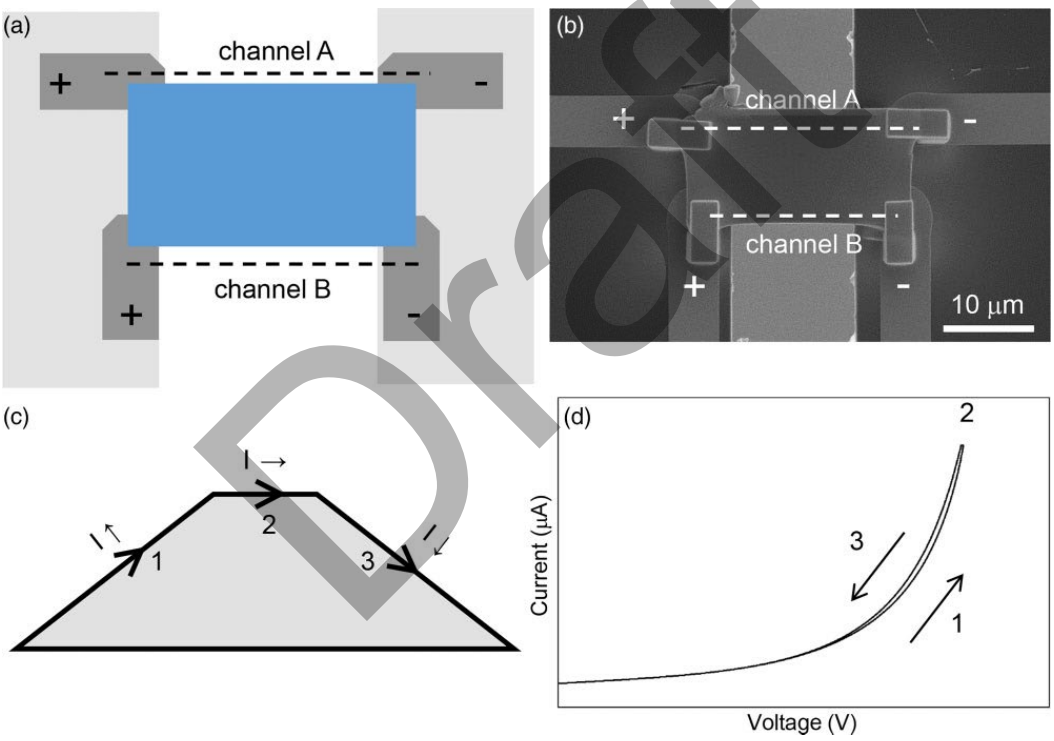

Fig. 3. A sketch (a) and an SEM image (b) of a lamella attached to the FIB-optimized E-chip. The measurement procedure was conducted in a 3-step waveform mode (c, d).[3]

Using this setup, the influence of different parameters on the current–voltage characteristics were evaluated, from the size of Pt contacts, incident Ga-beam energy, the electron-beam exposure of the Pt deposits, lamella thickness and specific design of the specimen geometry [3].

Conclusions

We report a detailed protocol for the FIB sample preparation of TEM lamellae on MEMS-based chips for in-situ electrical and electro-thermal TEM experiments that optimises the contact resistances. For the introduced methodology, a FIB instrument with a micromanipulator, one custom flat holder and one custom holder with a tilt (FIB-optimized E-chip), or two custom flat holders (E-chips with a membrane) are required. For optimal results, a FIB-optimized E-chip is favourable. An alternative geometry used for the lift-out procedure of the lamella provides a special benefit, where the lamella is directly fixed to the E-chip, without using an intermediate attachment to the grid. The proposed method is suited for any material that can undergo a regular FIB preparation procedure. High-resolution STEM imaging combined with analytical methods indicates a superb sample quality, especially of lamellae prepared on the FIB-optimized E-chip.

Based on our current–voltage characteristic measurements, there is only a minor, insignificant impact due to the beam energy during deposition or the size of the Pt contacts. Still, the contacts should be large enough to ensure a mechanical stability of the sample, especially when applying external stimuli. It is essential to mention the importance of refraining from immediate imaging after Pt deposition procedures, in order to avoid unnecessary Pt contamination of the chip/lamellae surface. It should be noted that the lamellae thickness influences systematically the measured current–voltage characteristics. Thinning of the whole lamella or parts of the lamella, as well as forming/cutting different slits into the lamella might influence the electrical characteristics and need to be carefully considered for each specific case.

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